REMARKS/ARGUMENTS

Claims 1, 3, and 5 are amended herein. Claim 9 is added herein. Claims 1-9 remain in the application. No new matter has been added. Consideration and examination is respectfully requested.

1. OBJECTION TO DRAWINGS:

In item 2 on page 2 of the Office Action dated 7 May 2004 (Paper No./Mail Date 3) referred to hereinafter as Paper 3, the drawings were objected to allegedly "because the functional blocks in FIG. 4 require appropriate legends describing the particular function without referring back to the specification."

Figure 4 has been modified in response to the instructions of Paper 3. A replacement sheet for Figure 4 and an annotated sheet showing the changes are attached hereto in the Appendix. Thus, Applicant has overcome the objection in item 2 of Paper 3.

2. OBJECTION TO SPECIFICATION:

In item 3 on page 2 of Paper 3, the specification was objected to allegedly "because the abstract of the disclosure does not comply with proper language and format."

The Abstract has been modified in response to the instructions of Paper 3. Thus, Applicant has overcome the objection in item 3 of Paper 3.

3. OBJECTIONS TO CLAIMS (CLAIMS 1-7):

In item 4 on page 3 of Paper 3, claims 1-7 were objected to allegedly "because they require indentation." Paper 3 stated that "Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation." Applicant respectfully traverses the objection.

Claims 2-4, 6, and 8 do not require indentation as they do not comprise a plurality of elements or steps. Claims 1, 5, and 7 are written with appropriate line indentations in the above "Amendments to the Claims" section. Thus, Applicant has overcome the objection in item 4 of Paper 3.

4. REJECTION OF CLAIMS 1-8 UNDER U.S.C. § 112:

In item 5 on page 3 of Paper 3, claims 1-8 were rejected under 35 U.S.C. § 112 "as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention."

Regarding Rejection of Independent Claim 1 Under 35 U.S.C. § 112:

Claim 1 was rejected for having insufficient antecedent basis for the following limitations in the claims: (1) "each input/output circuit", (2) "of the self-test data comparisons" and (3) "of the self-test". Applicant has appropriately modified claim 1 to provide such antecedent basis. Thus, Applicant has overcome the rejection of claim 1 in item 5 of Paper 3.

Regarding Rejection of Dependent Claims 2-8 Under 35 U.S.C. § 112:

Claims 2-8 were rejected to because they depend upon a main rejected claim. Since the rejection of claim 1 has been overcome, the rejection of dependent claims 2-8 has also been overcome.

5. REJECTION OF CLAIMS 1-6 & 8 UNDER U.S.C. § 102(e):

In item 6 on page 3 of Paper 3, claims 1-6 and 8 were rejected under 35 U.S.C. § 102(e) as being anticipated by Bhavsar et al. in U.S. Patent Number 6,408,401 entitled "Embedded RAM with Self-Test and Self-Repair with Spare Rows and Columns" hereinafter *Bhavsar*. Applicant respectively traverses.

As stated in MPEP 2131 "To anticipate a claim, the reference must teach every element of the claim." As will be shown in the following paragraphs, *Bhavsar* fails to teach every element of claims 1-6 and 8.

Regarding Rejection of Independent Claim 1 Under 35 U.S.C. § 102(e):

Among other items, *Bhavsar* does not disclose a control circuit "embedded in a control and address block of a RAM circuit" which is an element of claim 1 of the Present Application. *Bhavsar* discloses "Logic **201** for performing a self-test and self-repair algorithm also resides on the chip **12**, and communicates with the RAM **80** via the memory bus **20**." (*Bhavsar*: column 4, lines 14-16), but does not disclose a control circuit "embedded in a control and address block of a RAM circuit" as in claim 1. Figure 1 of *Bhavsar* shows logic **201** remotely located from RAM cache **80** and communicating with RAM cache **80** via memory bus **20** but does NOT show logic **201** embedded in the RAM cache **80**.

Thus, Applicant has demonstrated that *Bhavsar* fails to teach every element of claim 1. Because *Bhavsar* fails to teach every element of claim 1 as required by MPEP 2131, *Bhavsar* does not anticipate claim 1. In addition, *Bhavsar* fails to suggest every element of claim 1. Thus, claim 1 is allowable over *Bhavsar*.

Regarding Rejection of Dependent Claim 2 Under 35 U.S.C. § 102(e):

In the third paragraph on page 5, Paper 3 alleges that "*Bhavsar* discloses an electronic circuit 201 embedded in a RAM circuit chip 12 in an integrated circuit." Regardless, *Bhavsar*, among other items, does NOT disclose an electronic circuit "embedded within the RAM circuit" as is claimed in claim 2 of the Present Application. In *Bhavsar* "each chip **12** comprises some core logic **16**, which may contain, for example, arithmetic or floating point logic units and registers. In addition, each chip comprises an on-chip RAM cache **80**." (*Bhavsar*: column 4, lines 5-8). *Bhavsar* does NOT disclose an electronic circuit analogous to that of the Present Application in the RAM cache 80.

In addition, because dependent claim 2 depends from independent claim 1, it is noted that dependent claim 2 has all the features described above for claim 1 as elements. As demonstrated above, independent claim 1 is not anticipated by *Bhavsar*, nor does *Bhavsar* suggest every element of claim 1.

Thus, Applicant has demonstrated that *Bhavsar* fails to teach every element of claim 2. Because *Bhavsar* fails to teach every element of claim 2 as required by MPEP 2131, *Bhavsar* does not anticipate claim 2. In addition, *Bhavsar* fails to suggest every element of claim 2. Thus, claim 2 is allowable over *Bhavsar*.

Regarding Rejection of Dependent Claim 3 Under 35 U.S.C. § 102(e):

In the fourth paragraph on page 5, Paper 3 alleges that "*Bhavsar* discloses a control circuit (RAM Test Algorithm Engine 207) and address selection circuit (Address and

Read/Write Data path logic 255), which are embedded in a control and address block of the RAM circuit chip 12." Applicant notes that Paper 3 failed to identify which element disclosed in *Bhavsar* was considered to be analogous to the control and address block of the RAM circuit of claim 3 of the Present Application. As such it is difficult, if not impossible, for Applicant to fully address this rejection. However, Applicant notes that in Figure 2 the RAM Test Algorithm Engine **207** is included in logic **201**, whereas the Address and Read/Write Data Path Logic **255** is a part of the RAM segment **251**. The only common container within which the RAM Test Algorithm Engine **207** and the Address and Read/Write Data path logic **255** reside appears to be the chip **12** NOT a control and address block of the RAM circuit. Thus, in addition to other items, claim 3 differs from *Bhavsar* as indicated above.

In addition, because dependent claim 3 depends from independent claim 1, it is noted that dependent claim 3 has all the features described above for claim 1 as elements. As demonstrated above, independent claim 1 is not anticipated by *Bhavsar*, nor does *Bhavsar* suggest every element of claim 1. For this and other reasons, claim 3 differs from *Bhavsar*.

Thus, Applicant has demonstrated that *Bhavsar* fails to teach every element of claim 3. Because *Bhavsar* fails to teach every element of claim 3 as required by MPEP 2131, *Bhavsar* does not anticipate claim 3. In addition, *Bhavsar* fails to suggest every element of claim 3. Thus, claim 3 is allowable over *Bhavsar*.

Regarding Rejection of Dependent Claim 4 Under 35 U.S.C. § 102(e):

Because dependent claim 4 depends from independent claim 1, it is noted that dependent claim 4 has all the features described above for claim 1 as elements. As demonstrated above, independent claim 1 is not anticipated by *Bhavsar*, nor does *Bhavsar* suggest every element of claim 1. For this and other reasons, claim 4 differs from *Bhavsar*.

Thus, Applicant has demonstrated that *Bhavsar* fails to teach every element of claim 4. Because *Bhavsar* fails to teach every element of claim 4 as required by MPEP 2131, *Bhavsar* does not anticipate claim 4. In addition, *Bhavsar* fails to suggest every element of claim 4. Thus, claim 4 is allowable over *Bhavsar*.

Regarding Rejection of Dependent Claim 5 Under 35 U.S.C. § 102(e):

Because dependent claim 5 depends from independent claim 1, it is noted that dependent claim 5 has all the features described above for claim 1 as elements. As demonstrated above, independent claim 1 is not anticipated by *Bhavsar*, nor does *Bhavsar* suggest every element of claim 1. For this and other reasons, claim 5 differs from *Bhavsar*.

Thus, Applicant has demonstrated that *Bhavsar* fails to teach every element of claim 5. Because *Bhavsar* fails to teach every element of claim 5 as required by MPEP 2131, *Bhavsar* does not anticipate claim 5. In addition, *Bhavsar* fails to suggest every element of claim 5. Thus, claim 5 is allowable over *Bhavsar*.

Regarding Rejection of Dependent Claim 6 Under 35 U.S.C. § 102(e):

In the last paragraph on page 6, Paper 3 alleges that "*Bhavsar* discloses an address multiplexer (95 and 96), register (304 and 302), sequencer (counter 330) and comparator (XOR 98), which are all embedded in a control and address block of the RAM circuit chip 12, FIG. 1." Applicant notes that Paper 3 again failed to identify which element disclosed in *Bhavsar* was considered to be analogous to the control and address block of the RAM circuit of claim 6 of the Present Application. As such it is difficult, if not impossible, for Applicant to fully address this rejection.

In addition, because dependent claim 6 depends from independent claim 1 via dependent claim 5, it is noted that dependent claim 6 has all the features described above for

claims 1 and 5 as elements. As demonstrated above, independent claim 1 is not anticipated by *Bhavsar*, nor does *Bhavsar* suggest every element of claim 1. For this and other reasons, claim 6 differs from *Bhavsar*.

Thus, Applicant has demonstrated that *Bhavsar* fails to teach every element of claim 6. Because *Bhavsar* fails to teach every element of claim 6 as required by MPEP 2131, *Bhavsar* does not anticipate claim 6. In addition, *Bhavsar* fails to suggest every element of claim 6. Thus, claim 6 is allowable over *Bhavsar*.

Regarding Rejection of Dependent Claim 8 Under 35 U.S.C. § 102(e):

Paper 3 rejected dependent claim 8 under 35 U.S.C. § 102(e) but did not reject claim 7 upon which claim 8 depends. Because dependent claim 8 depends from dependent claim 7, it is noted that dependent claim 8 has all the features described above for claim 7 as elements. Since claim 7 has not been rejected as being anticipated by *Bhavsar*, claim 8 comprises elements which Paper 3 did not identify as being taught by *Bhavsar*. Thus, *Bhavsar* does not anticipate, nor does *Bhavsar* suggest every element of claim 8.

In addition, because dependent claim 8 depends from independent claim 1 via dependent claim 7, it is noted that dependent claim 8 has all the features described above for claim 1 as elements. As demonstrated above, independent claim 1 is not anticipated by *Bhavsar*, nor does *Bhavsar* suggest every element of claim 1. For this and other reasons, claim 8 differs from *Bhavsar*.

Thus, Applicant has demonstrated that *Bhavsar* fails to teach every element of claim 8. Because *Bhavsar* fails to teach every element of claim 8 as required by MPEP 2131, *Bhavsar* does not anticipate claim 8. In addition, *Bhavsar* fails to suggest every element of claim 8. Thus, claim 8 is allowable over *Bhavsar*.

6. REJECTION OF CLAIM 7 UNDER 35 U.S.C. § 103(a):

In item 7 on page 7 of Paper 3, claim 7 was rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over *Bhavsar* in view of Gupta et al. in U.S. Patent Number 6,609,222 entitled "Methods and Circuitry for Built-In Self-Testing of Content Addressable Memories" hereinafter *Gupta*. Applicant respectfully traverses.

> Referring to MPEP 2142, "To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations."

Regarding Rejection of Claim 7 Under 35 U.S.C. § 103(a):

With respect to the rejection of claim 7 under 35 U.S.C. § 103(a), it is noted that dependent claim 7 depends from independent claim 1 and that, as such, dependent claim 7 has all the features described above for claim 1 as elements. As demonstrated above, among other items, *Bhavsar* does not disclose a control circuit "EMBEDDED in a control and address block of a RAM circuit" which is an element of claim 1 of the Present Application.

Thus, the cited reference does not teach nor does it suggest all the claim limitations of claim 7 as required by MPEP 2142. As such, claim 7 is not obvious over *Bhavsar*, and it follows that claim 7 is allowable.

7. IN CONCLUSION:

Entry of this amendment is respectfully requested. Applicant believes that all claims pending in the Present Application as described above are allowable and that all other issues raised by the Examiner have been rectified. Therefore, Applicant respectfully requests the Examiner to reconsider his rejections and to grant an early allowance.

Respectfully submitted,

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APPENDIX

The attached following sheets of drawings includes changes to Figure 4. The first sheet is a replacement sheet for sheet 4 (Figure 4), and the second is an annotated sheet 4 showing handwritten changes to Figure 4.